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FIGURE 1A

100

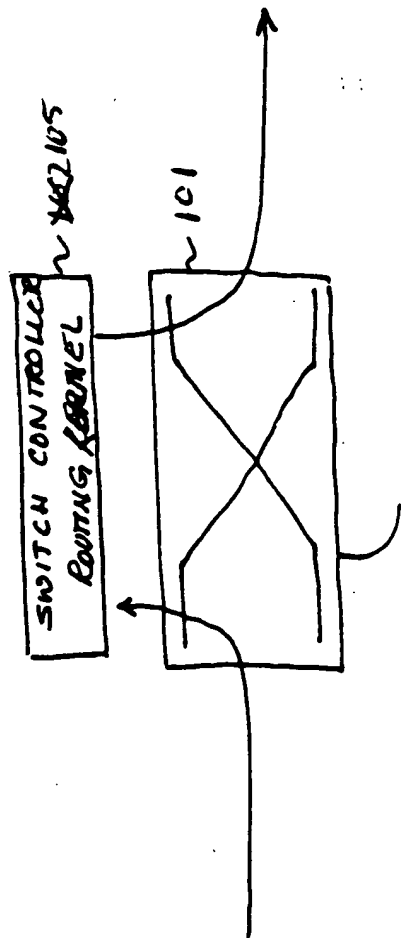
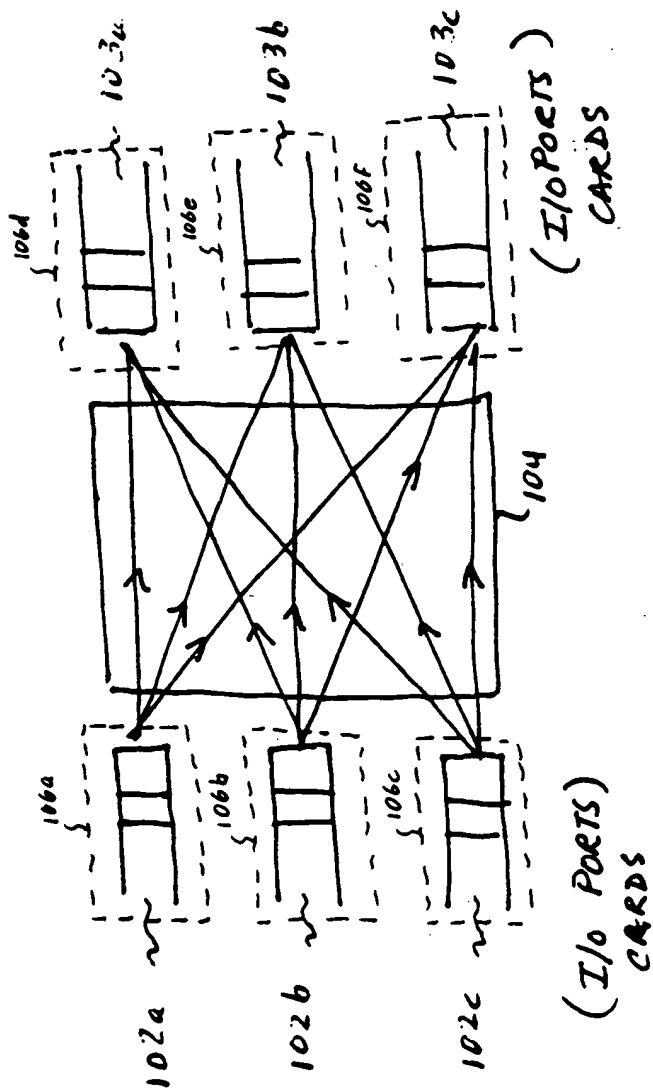


FIG. 1B is a schematic diagram of a system architecture showing a central processing unit (104) connected to two sets of I/O ports (102a, 102b, 102c and 103a, 103b, 103c) via a network of lines (106a, 106b, 106c, 106d, 106e, 106f). The I/O ports are labeled (I/O PORTS) CARDS.

FIG. 1B

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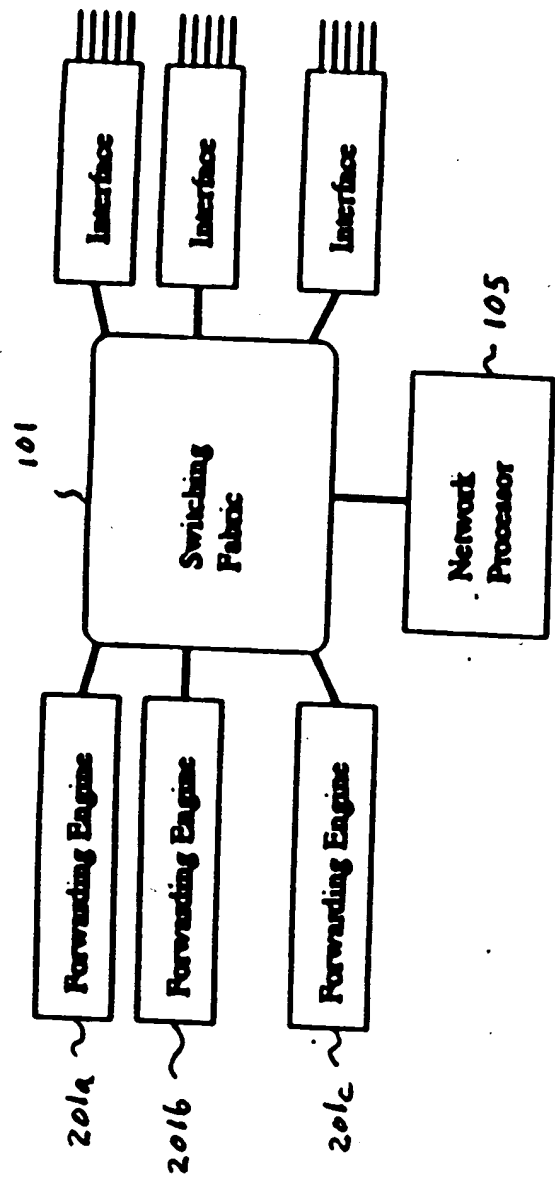


FIG. 2A

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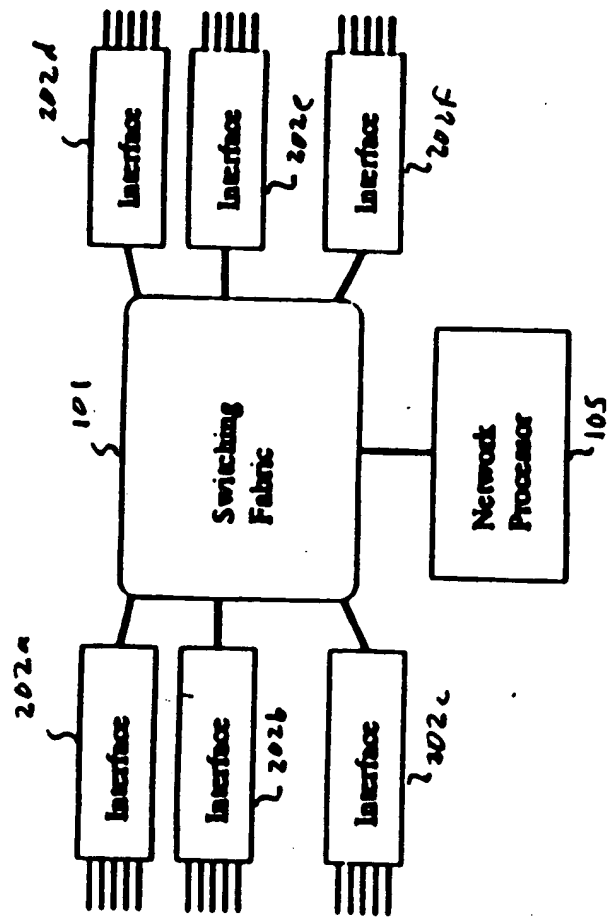


Figure 2B

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FIGURE 3.

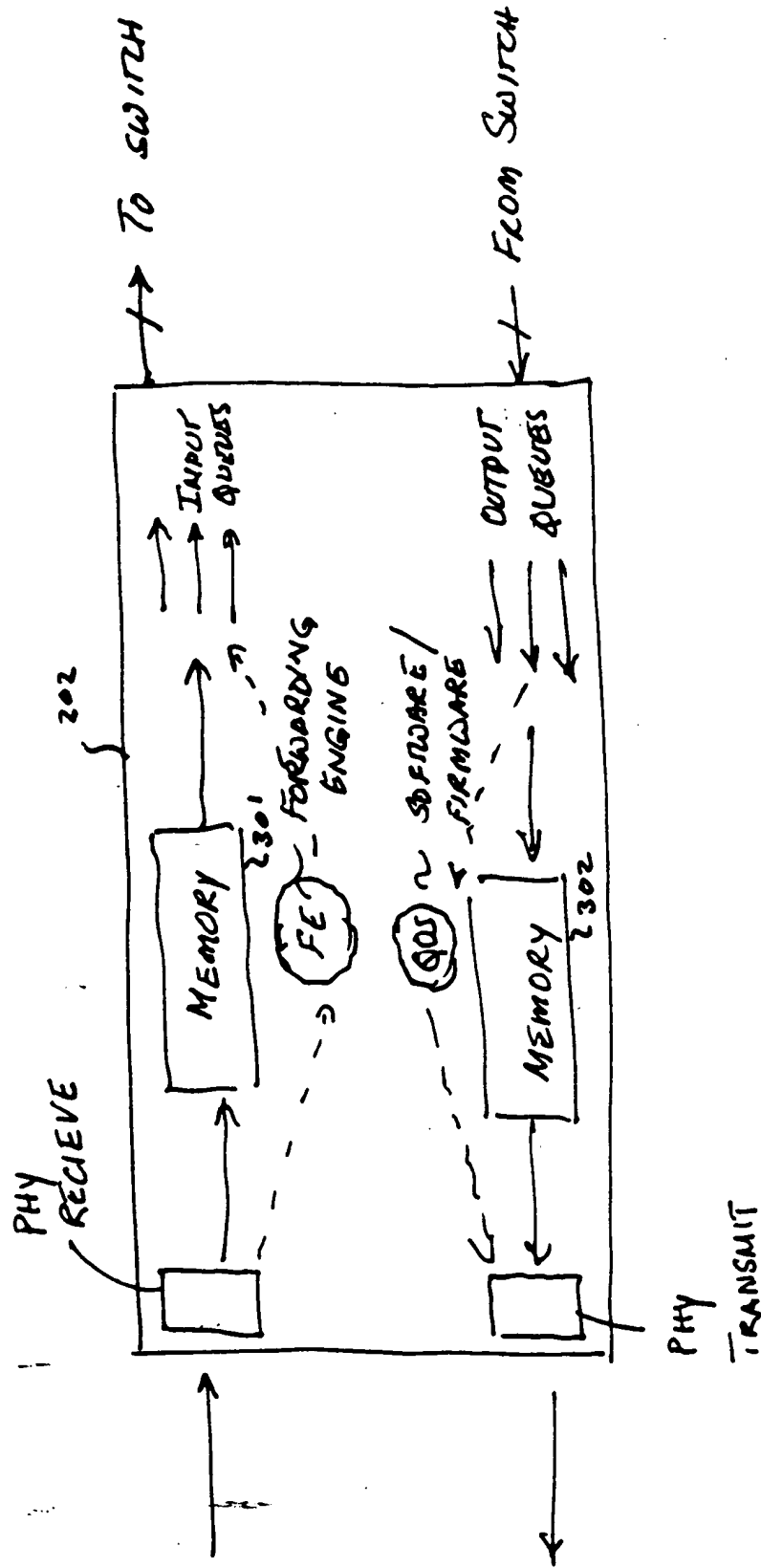


FIGURE 4A

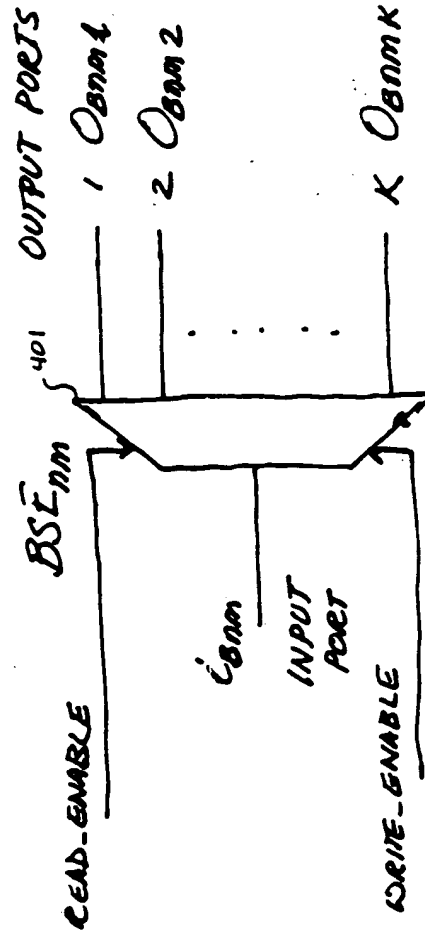
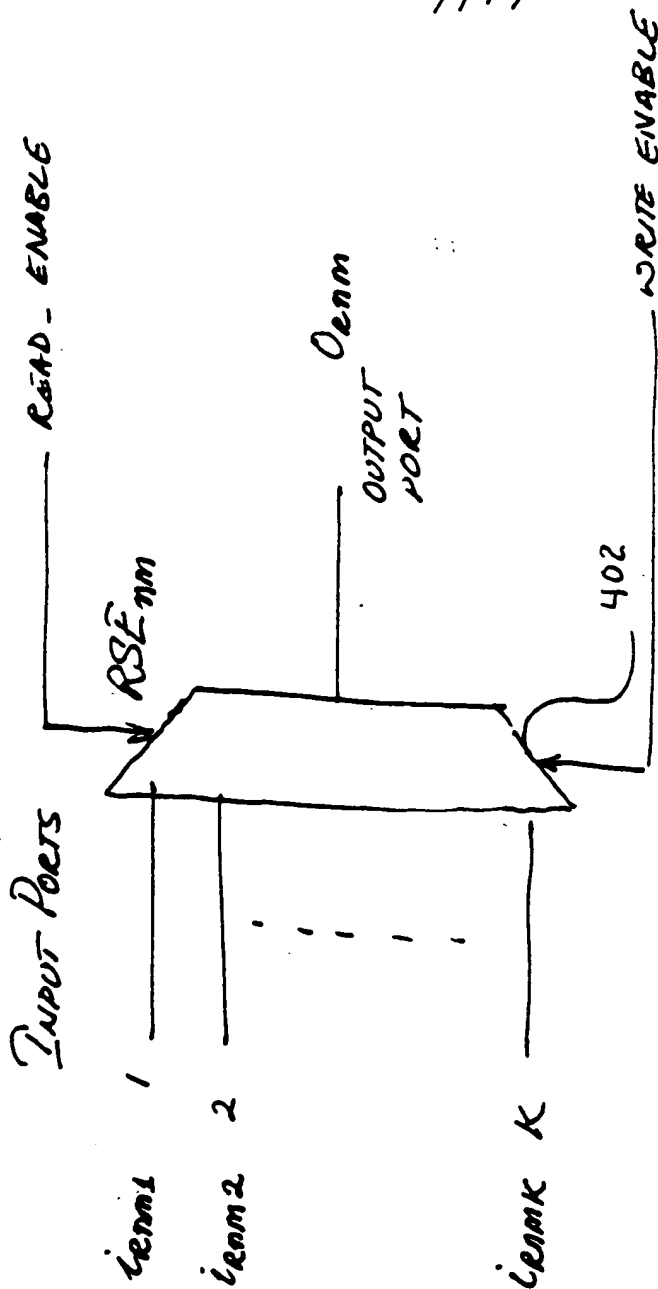


FIGURE 4B



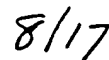
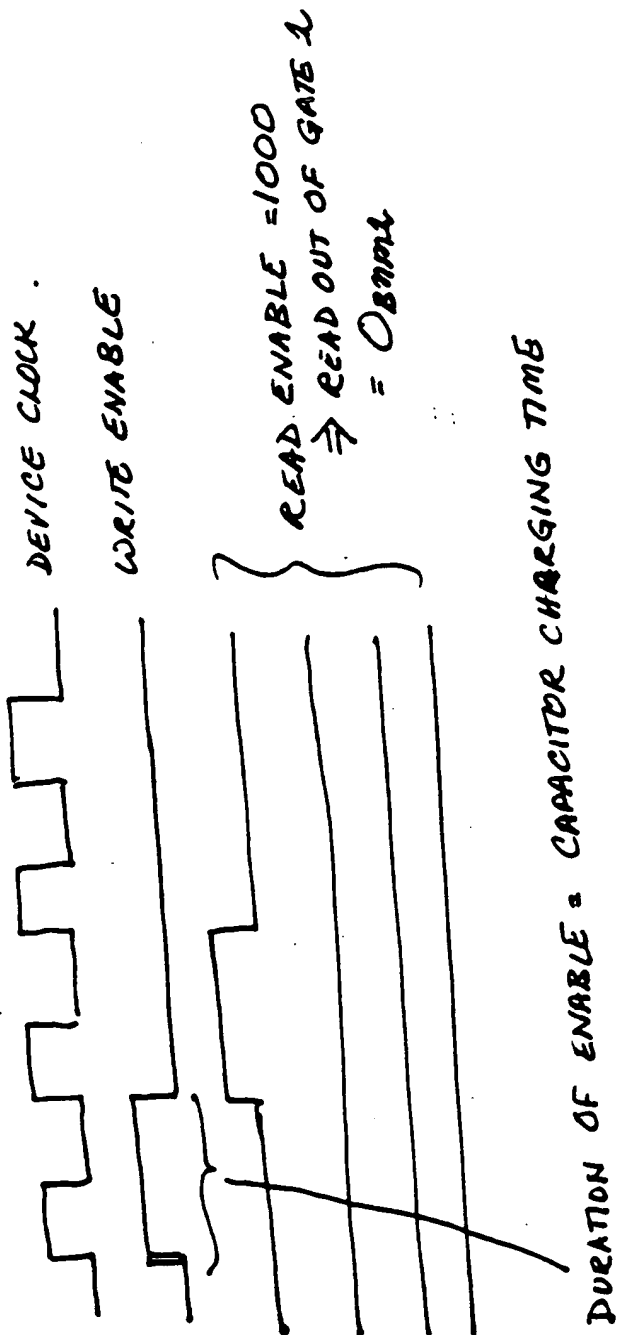
[illegible]



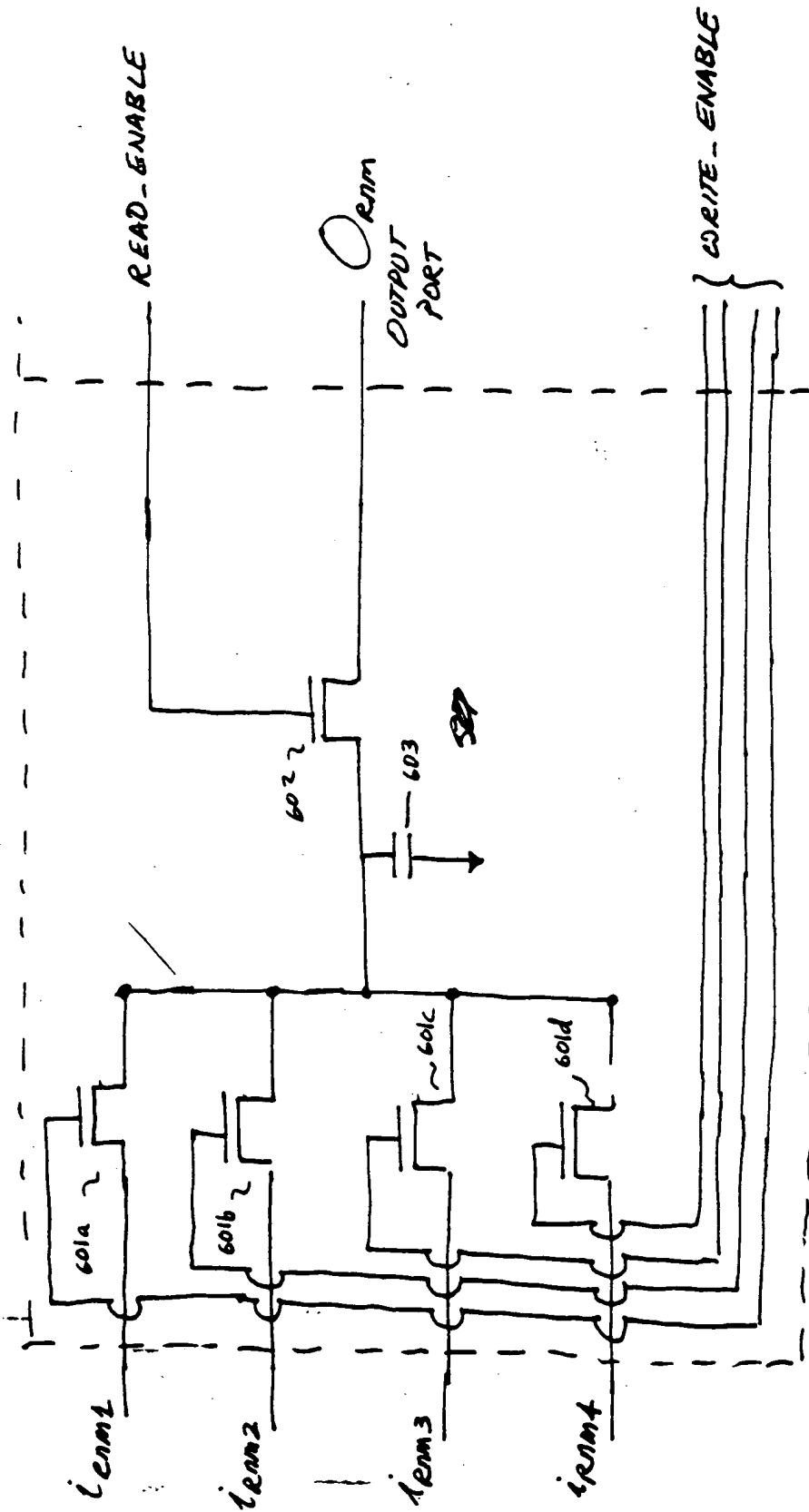
FIGURE 5B



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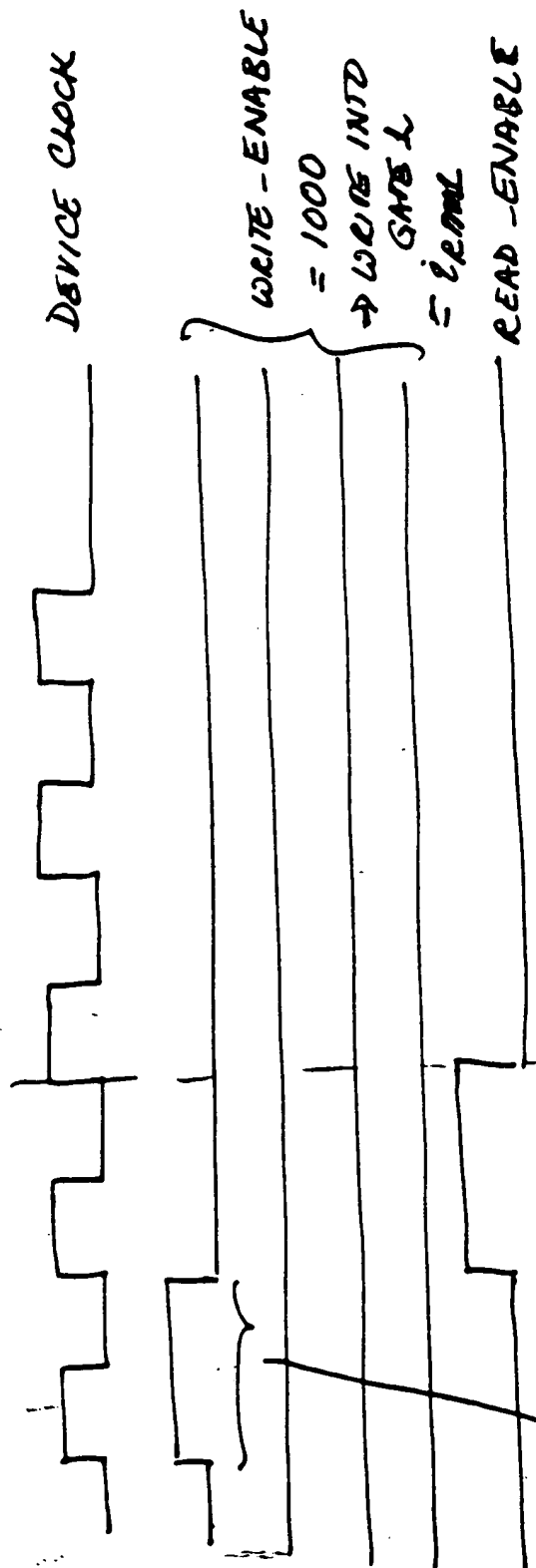
FIGURE 6A

INPUT PORTS



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Figure 6B



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FIG. 7

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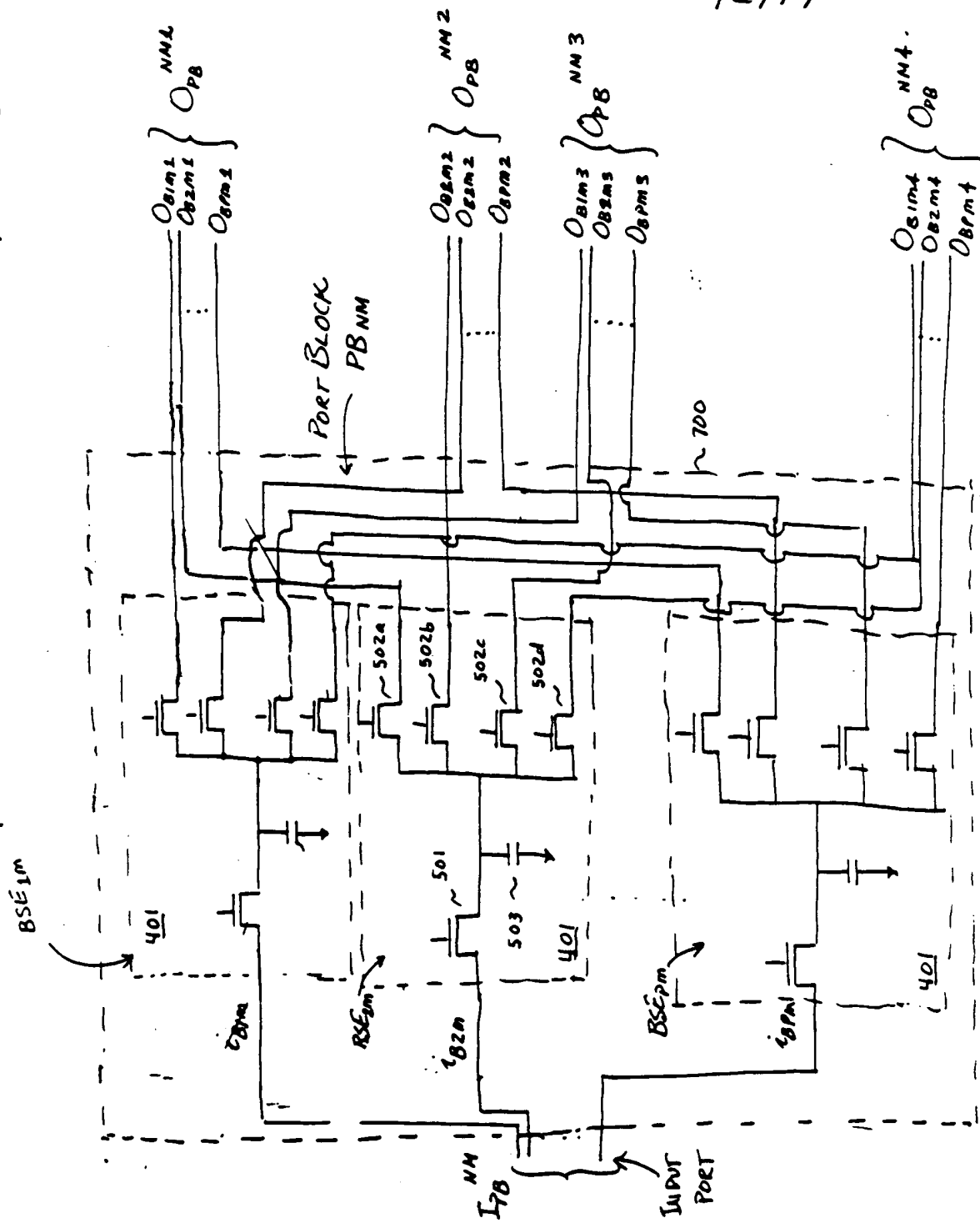
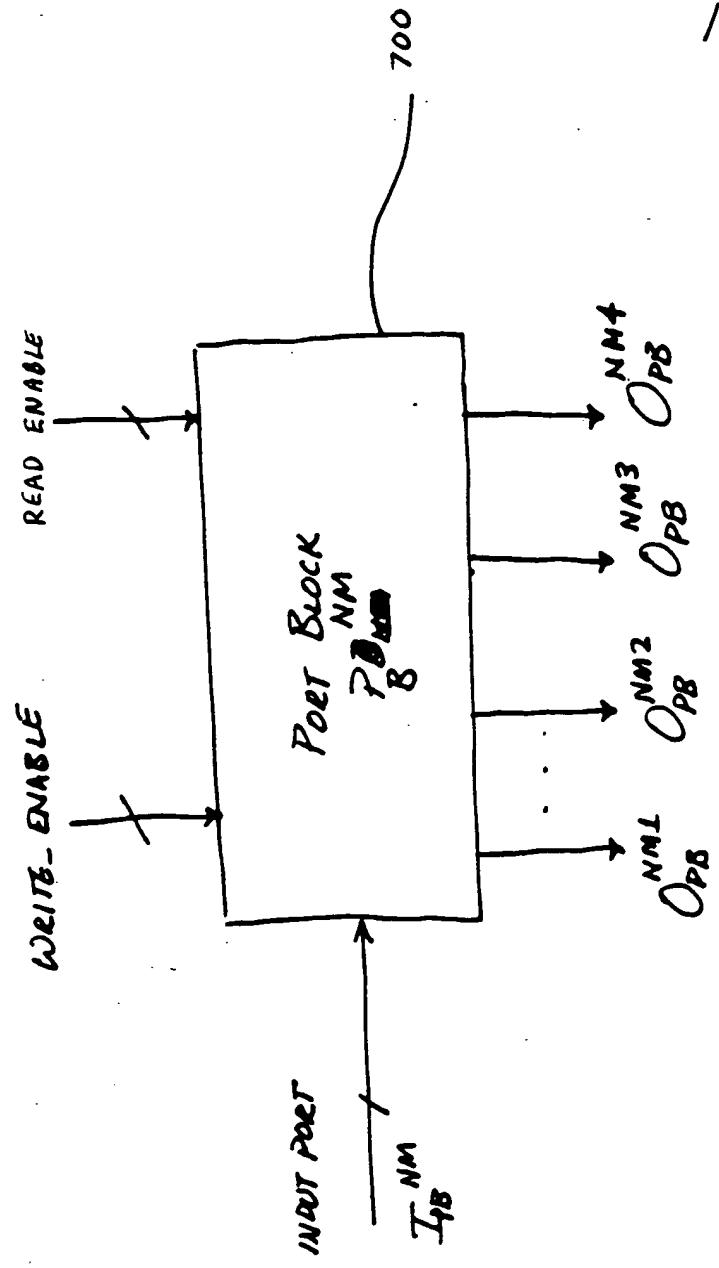
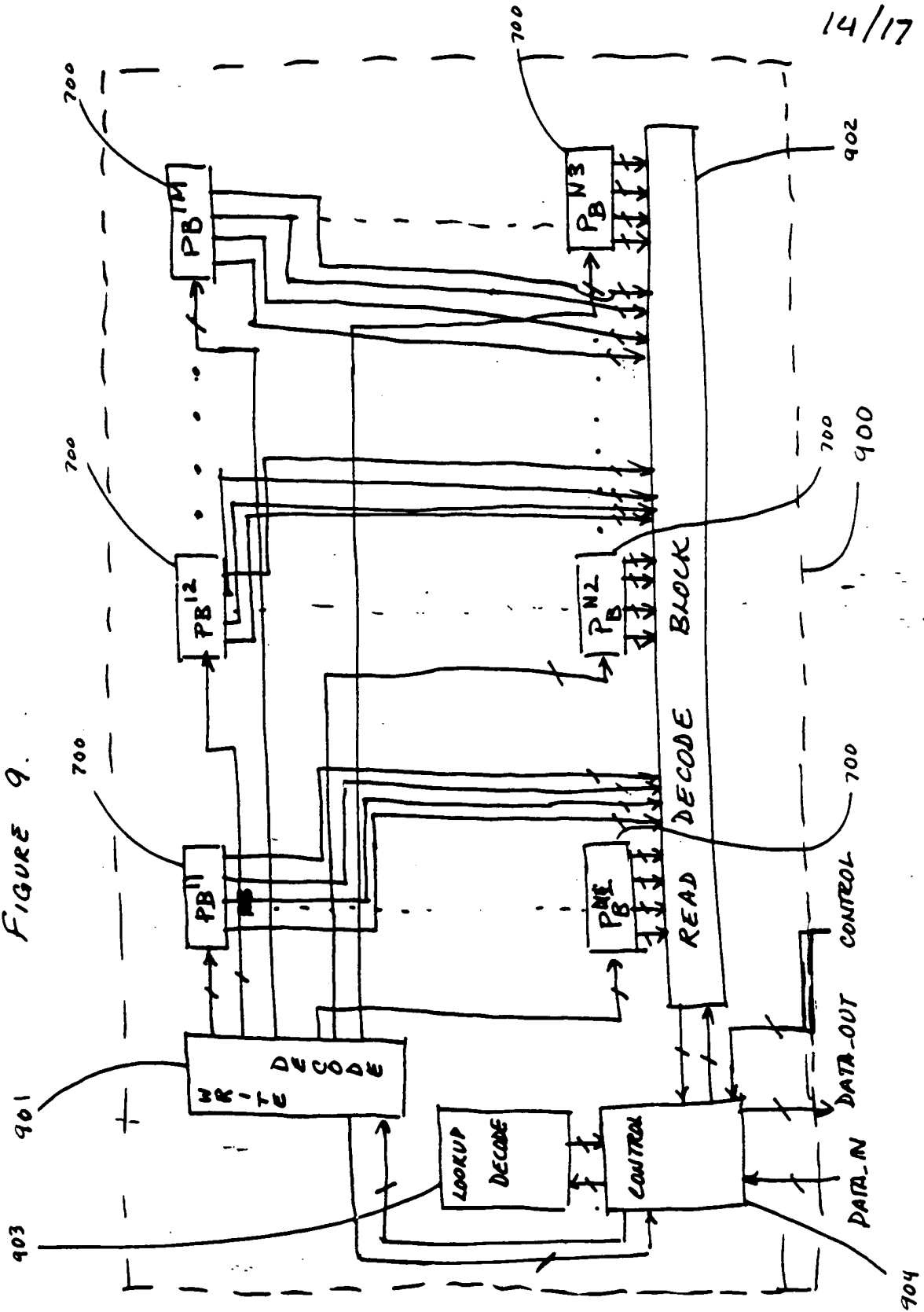


FIGURE 8



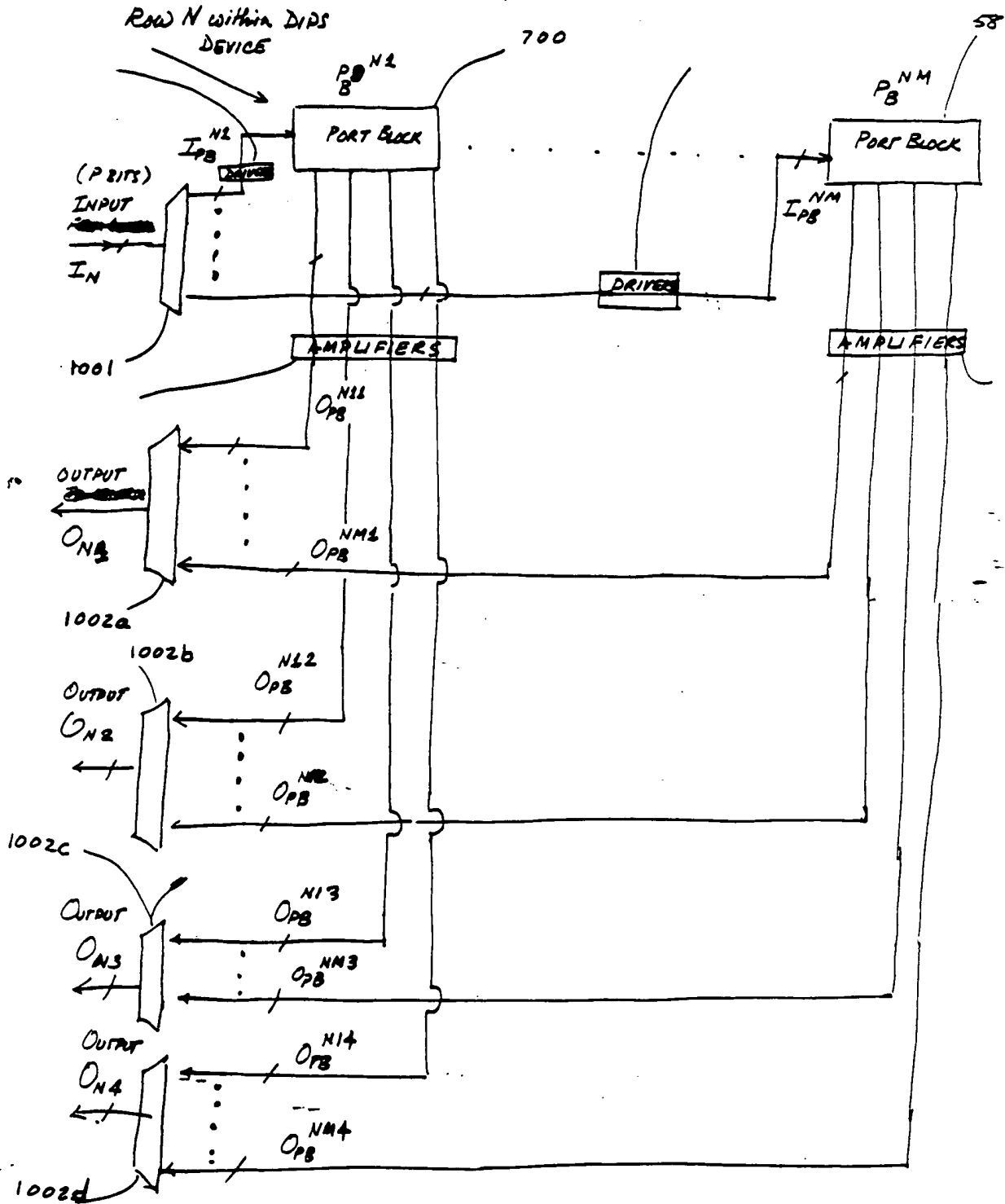
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FIGURE 9.



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FIGURE 10.



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FIG. 11A

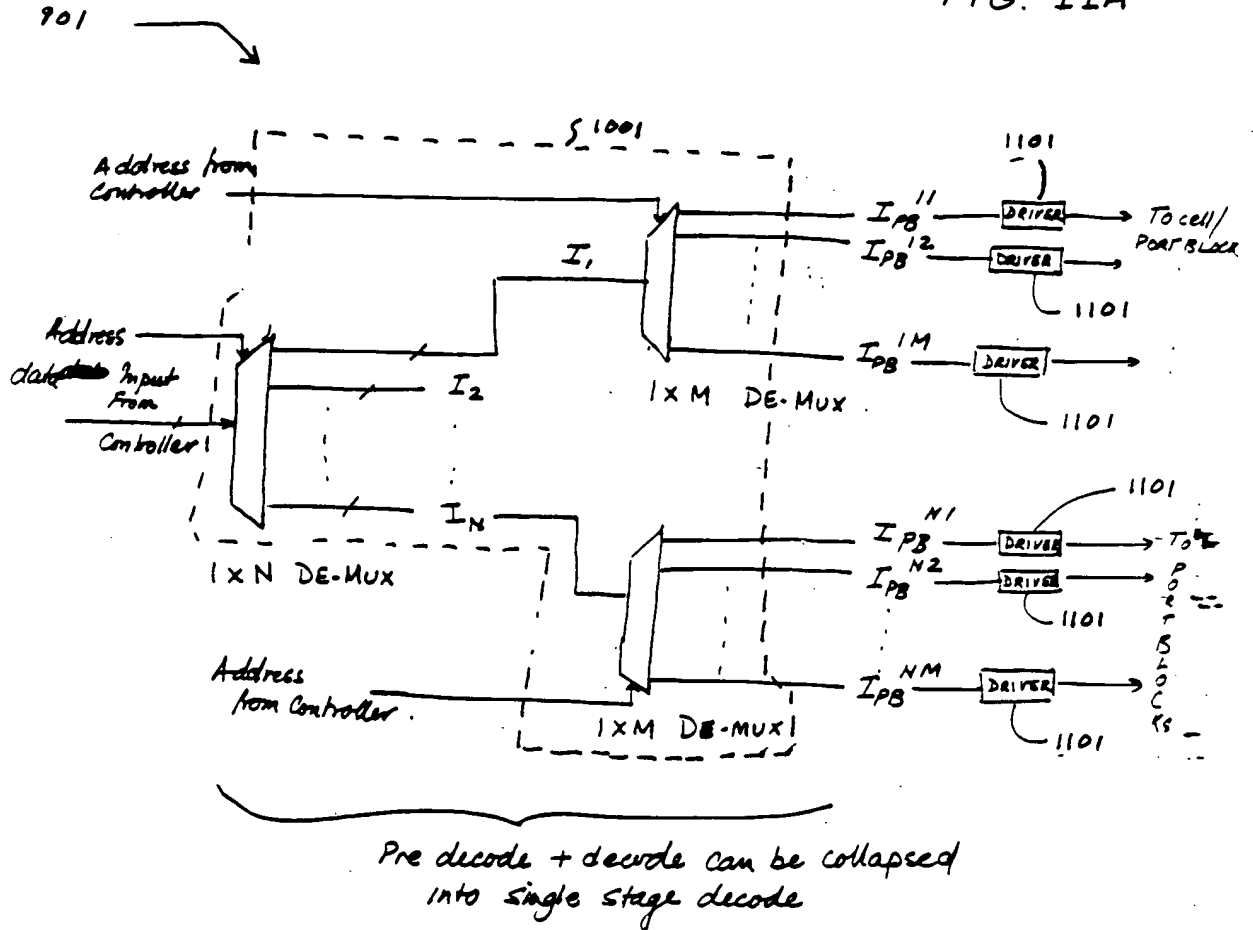


FIGURE 11B

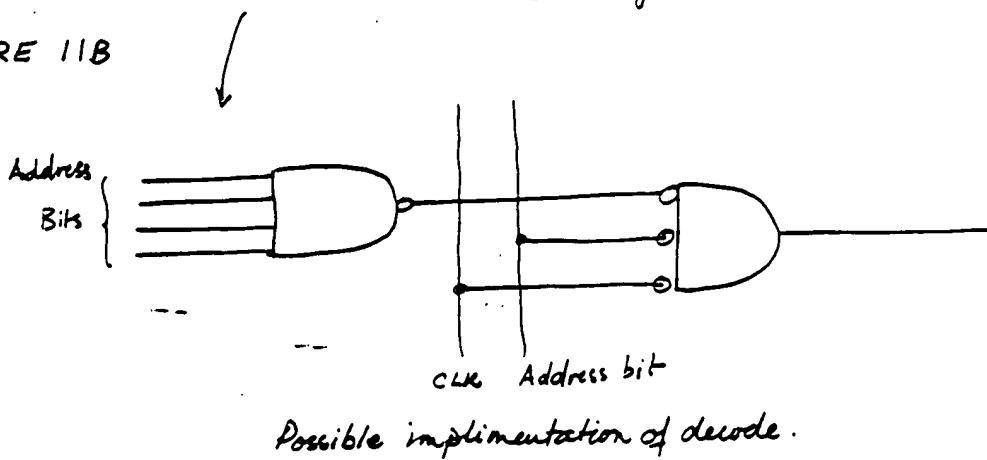




FIGURE 2.

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